A 7 WATT C-BAND FET AMPLIFIER USING SERIAL POWER COMBINING TECHNIQUES

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ABSTRACT

This paper describes the development of a 7 watt FET amplifier operated in the satellite communication band (3.7 GHz to 4.2 GHz) using serial power combining techniques. This three-stage MIC power amplifier provides 16.6 dB power gain, 33.1% power added efficiency, and over 500 MHz 1 dB bandwidth. The FET power amplifier features good efficiency, low noise figure, and excellent linearity. It is an ideal solid state replacement for the traveling wave tube amplifier in future communication systems.

Introduction

Modern communication systems require high power solid state amplifiers with good dc-RF conversion efficiency, low intermodulation distortion, and high reliability. With the advancement of GaAs device technology,[1,2] GaAs field effect transistors with power capability of several watts are presently available at the C-band frequency. By combining several FET amplifiers at the output stage, the solid state FET amplifier can be used to replace TWTA's in future communication systems.[3] Serial power combining techniques were developed for the final stage of this power amplifier chain, as shown in the circuit block diagram of Figure 1. The major advantage of this form of power combining lies in its ability to produce non-binary power combining and dividing. With the serial power combining, any odd or even number of amplifiers can be combined. Therefore, the serial power combining techniques provide an economical way to achieve the required output power with the minimum number of active devices.

Device Characterization and Amplifier Design

The active devices used in this amplifier, Fujitsu's high power field effect transistors FLC-30 and FLC-15, are commercially available. The FLC-30 has a gate length of 1.5 μm with total gate width of 5200 μm, which provides 2.5 watts output power at 4 GHz. The FLC-15 is half the size of the FLC-30, delivers 1.25 watts output power at the same frequency.

In designing the single stage high power broadband amplifier, the small signal S-parameters that help determine the small signal gain and stability criteria of the device were measured first. The optimum impedance contours for the high power and the high efficiency operation were then obtained by the substitution method. With the large signal characteristics of the FET, high power broadband amplifiers were then designed and constructed on 25-mil-thick alumina substrate.

Usually, microwave matching circuits and dc bias circuits tend to present a very high or very low impedance at the out-of-band frequency. Both FLC-30 and FLC-15 are conditionally stable for frequencies below 3 GHz. Therefore, it is important to choose the proper RF matching circuit and dc bias circuit to provide stable operating conditions at all the frequencies. In this design, stabilization circuits are used at both the gate bias and drain bias circuits to suppress the unwanted oscillation.

A single stage FLC-30 amplifier was built and tested for the driver. The FLC-30 amplifier gives 2.5 watts output power with 5.1 dB gain at 3.9 GHz. The 1 dB bandwidth of this amplifier is 750 MHz, and the power added efficiency is 37.7%. For linear operation, the amplifier provides over 1 watt output power, with third order intermodulation distortion better than 30 dB down from the carrier. This amplifier was designed to provide a compromised performance between the amplifier power, bandwidth, efficiency, and linearity. With some adjustment of the matching circuits and biasing voltages, power added efficiency of 44% was achieved, with slight reduction (0.2 dB) in output power. The amplifier linearity can also be further improved with tradeoff in other parameters.

Three additional FLC-30 amplifiers were constructed and tested for the output stage. These amplifiers are extremely uniform in their performance. The maximum power variation between amplifiers is no more than 0.4 dB, with phase variation less than 10° from amplifier to amplifier.

Serial Power Combining and Dividing Circuits

Serial power combination consists of several serial cascaded couplers that provide equal power splitting among all the output ports. After amplification, the amplified signals are recombined by an identical set of couplers. For N-way serial power combining and dividing circuits, the couplers on the dividing side have an increasing power coupling coefficient that varies from 1/N to 1/2. On the combining side, the power coupling coefficient decreases in reverse order from 1/2 to 1/N, where N is the number of power amplifiers to be combined. Thus, a three-way serial combining system consists of a 4.77 dB coupler and a 3 dB coupler. A four-way system needs an additional 6 dB coupler at the input of the three-way system, and so on.

In order to achieve broad bandwidth and good isolation between amplifiers, the interdigitated couplers[4] were chosen for the three-way power combining circuit. The three-way power combining/dividing circuits were fabricated on 25-mil-thick alumina substrates with Cr-Cu-Au metallization. The coupling and isolation between the ports of the three-way power combining/dividing circuits are depicted in Figure 2. The average insertion loss of the three-way combining/dividing circuits is 0.35 dB over the frequency band of interest. The minimum isolation between the output ports is better than 25 dB. These low loss, high isolation, power combining/dividing circuits are extremely desirable for the power combining of the FET amplifiers.

Amplifier Performance

Figure 3 shows a photograph of the three-stage serial power combined FET amplifier. The amplifier weighs 12.8 ounces, with overall dimensions of 5" by 3" by 1". The frequency response of the completed amplifier is

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shown in Figure 4. At 22 dBm input power, the amplifier delivers 7.3 watts with better than 500 MHz 1 dB bandwidth. The overall power added efficiency is 33.1%. The power transfer characteristic and its harmonic contents are shown in Figure 5. The FET amplifier exhibits excellent power limiting capability. The output power varies less than 0.8 dB, with 15 dB overdrive beyond the 1 dB compression point. In the deep saturation region, the second and third harmonic powers stay relatively constant at 37 dB below the fundamental power level.

The intermodulation performance was measured with two equal amplitude carriers 2 MHz apart. Figure 6 depicts the results of the two tones measurement at 4 GHz. The third order intermodulation deteriorated rapidly as the output power approached 1 dB compression point. Beyond the saturation point, carrier to third order intermodulation ratio gradually improved to 29 dB. The amplifier has a maximum 1°/dB of AM to PM conversion for power levels below 1 dB compression point. The noise figure of this 7 watt power amplifier was measured and is shown in Figure 7. The maximum in-band noise figure is better than 4.5 dB, with a minimum noise figure of 3.9 dB at 3.9 GHz.

Excellent temperature stability (Figure 8) is demonstrated by this FET amplifier. The power output of the amplifier varies less than 0.4 dB (-5° to 55°C), with almost no change in overall power added efficiency. RF life test of this power amplifier chain has been initiated. The amplifier operates in ambient temperature of 27°C with no cooling mechanism provided. Over 2000 hours of RF operating life have been recorded with no degradation in the amplifier performance.

Conclusion

Excellent performance has been achieved with the solid state FET power amplifier. This FET amplifier delivers over 7 watts of output power at C-band frequency, with 16.6 dB power gain and 33.1% power added efficiency. The FET amplifier shows excellent overdriven capability and superior linearity compared to that of the TWT amplifier. The design of this three-stage FET amplifier compromises the power, bandwidth, efficiency, and linearity of the amplifier performance. Each individual characteristic of the FET amplifier can be further improved to meet specific system requirements.

Acknowledgement

The author wishes to thank M. D. Rubin for many valuable discussions, and H. Burdman and R. Mencik for their technical assistance.

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3. Ho, P. T., Rubin, M. D., and Wherry, J. G., "Solid State Amplifiers in Communications Satellites." The Seventh AIAA Communications Satellite Systems Conference, San Diego, California, April 1978.

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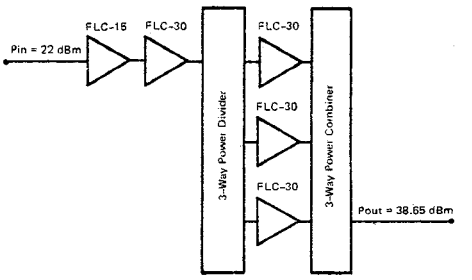

Figure 1. Circuit Block Diagram of the 7 Watt C-Band FET Amplifier

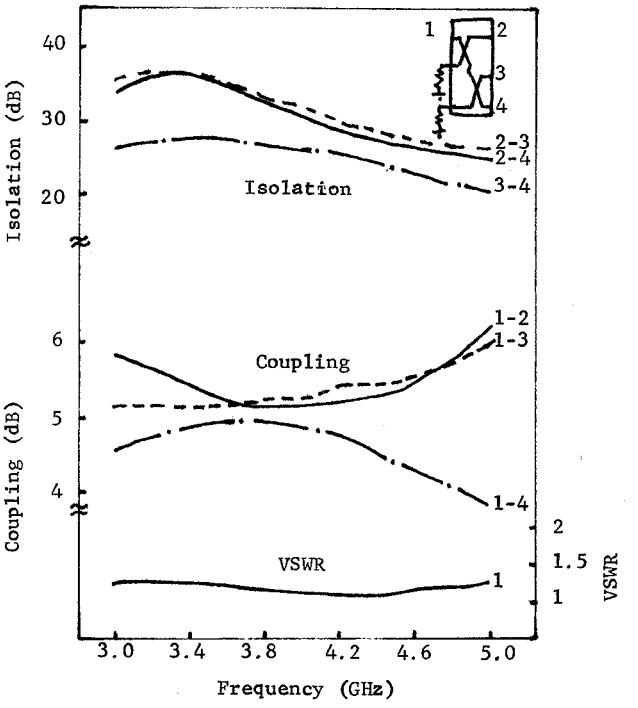

Figure 2. Performance of the Three-Way Serial Power Combining and Dividing Circuits

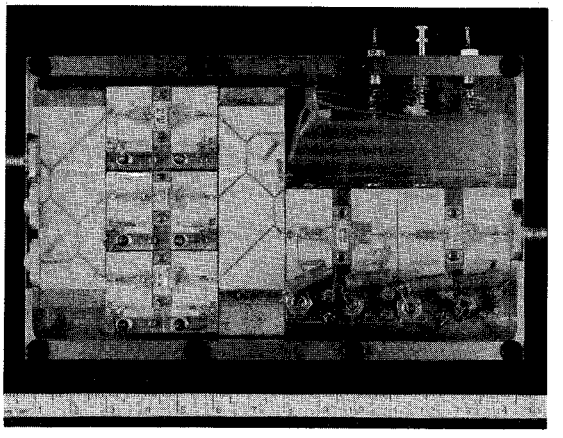

Figure 3. Photograph of the Completed 7 Watt, Three-Stage FET Amplifier

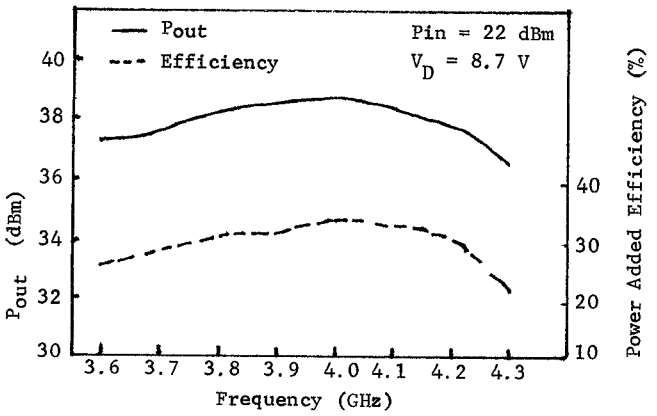

Figure 4. Frequency Response and Power Added Efficiency of the Three-Stage FET Amplifier

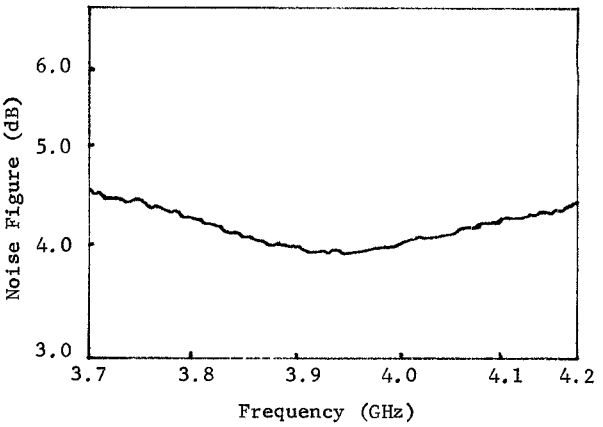

Figure 7. Noise Figure of the Three-Stage FET Amplifier

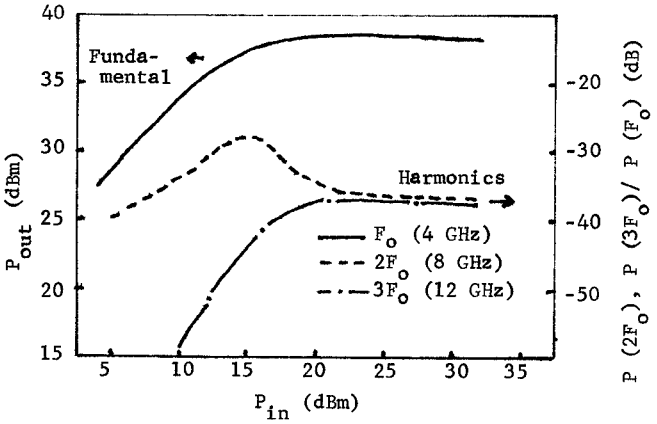

Figure 5. Power Transfer Characteristic and Harmonic Contents of the Three-Stage FET Amplifier

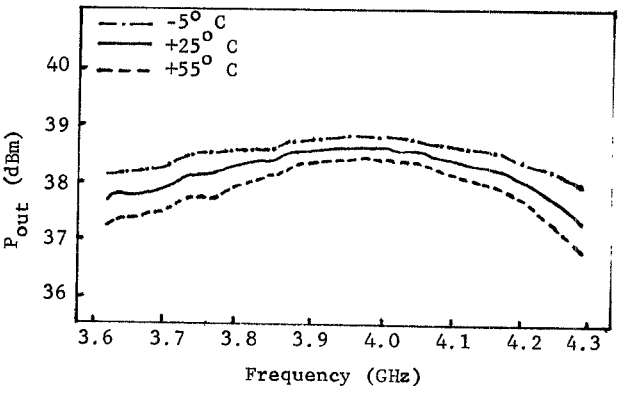

Figure 8. Saturated Power Output of the Three-Stage FET Amplifier Over Temperatures

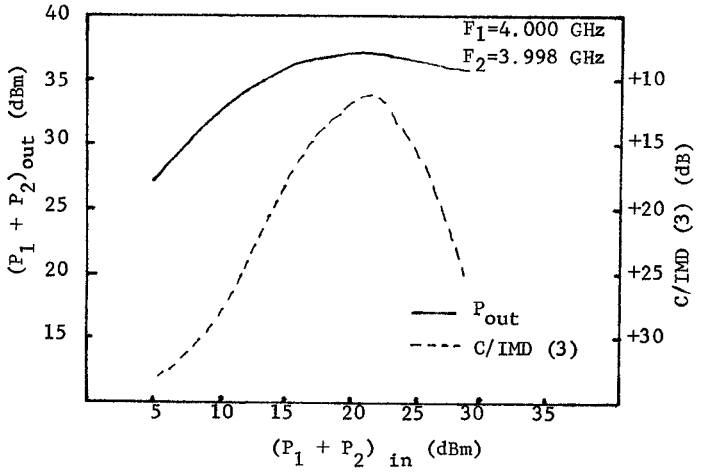

Figure 6. Two Tones Intermodulation Test of the Three-Stage FET Amplifier